

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("6574760").PN.	US_PGPUB; USPAT	OR	OFF	2008/12/21 22:53
S38	1	(executing second test concurrently) same (processing same first test or test data)	US_PGPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:34
S39	1	(executing second test concurrently) and (processing same first test or test data)	US_PGPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:34
S40	1	mixed signal semiconductor device and (wafer testing same package testing)	US_PGPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:43
S41	29	(wafer testing same package testing)	US_PGPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:43
S42	39	mixed signal semiconductor device	US_PGPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:43

S43	1	S41 and S42	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:43
S44	67	S41 or S42	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:43
S45	5425	((concurrently) or (parallel) or (simultaneously) or (at the same time)) and (first test same second test) or (S44)	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:45
S46	5360	((concurrently) or (parallel) or (simultaneously) or (at the same time)) and (first test same second test)	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:45
S47	2	S46 and S44	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:46
S48	67	S45 and S44	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:52

S49	43	execut\$3 and (test script\$1 same (first test or primary test))	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:54
S50	1	S48 and S49	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:54
S51	516	computational module\$1	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:54
S52	1	S48 and S51	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:54
S53	3471	test instruction	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:55
S54	26544	single processor	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:55

S55	12	mixed signal semiconductor device and (testing circuit or device under test or unit under test)	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:56
S56	12	S48 and S55	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:56
S57	1	S54 and S56	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:56
S58	14740	714/724-725,733-734,10,11,30,38,742,740,776,702/118;716/4. ccls.	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:56
S59	4	S56 and S58	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 11:57
S60	29	(wafer testing same package testing)	US_PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 13:51

S61	39	mixed signal semiconductor device	US-PCPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 13:51
S62	67	S60 or S61	US-PCPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 13:51
S63	5425	((concurrently) or (parallel) or (simultaneously) or (at the same time)) and (first test same second test) or (S62)	US-PCPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 13:51
S64	67	S63 and S62	US-PCPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 13:51
S65	12	mixed signal semiconductor device and (testing circuit or device under test or unit under test)	US-PCPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 13:51
S66	12	S64 and S65	US-PCPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2008/12/14 13:51
S67	1	("4672534").PN.	US-PCPUB; USPAT	OR	OFF	2008/12/14 15:56

S68	2	(("6920585") or ("6536006")).PN.	US-PPGPUB; USPAT	OR	OFF	2008/12/14 16:10
S69	0	mixed signal semiconductor device AND single processor AND first test AND second test AND device interface unit AND device under test AND device testing unit AND control unit AND processor AND operating system AND computational modules). clm.	US-PPGPUB; USPAT; USOOR	ADJ	ON	2008/12/14 16:24

12/21/08 10:57:32 PM

C:\Documents and Settings\pchung\My Documents\EAST\Workspaces\10614997.wsp